PROGRAMMABLE TRANSMIT SCSI EQUALIZATION

FIELD OF THE INVENTION

The present invention relates to a method and/or architecture for implementing transceivers generally and, more particularly, to programmable transmit SCSI equalization.

BACKGROUND OF THE INVENTION

Referring to FIG. 1, a schematic of a conventional current mode small computer systems interface (SCSI) universal low voltage differential (ULVD) driver 10 is shown. The driver 10 has a number of transistors labeled A–D, a driver 12, a current source 14, a current source 16, a positive output pin 18, a negative output pin 20 and a terminator 22. Input data is presented to the transistors A and C and the transistors B and D in a differential configuration. Conventional current mode SCSI ULVD drivers do not control output rise time of output differential waveforms.

It is generally desirable to provide a method and/or architecture that may overcome SCSI cable induced effects by providing a controlled rise time and synchronized buffers for precompensation.

SUMMARY OF THE INVENTION

The present invention concerns an apparatus comprising a first plurality of parallel switches and a second plurality of parallel switches. The first plurality of parallel switches may be configured to control a first voltage on a first output pin. The second plurality of parallel switches may be configured to control a second voltage on a second output pin. The first and second pluralities of parallel switches may be configured to provide rise time control of a differential waveform and be driven by a phased data signal.

The objects, features and advantages of the present invention include providing a method and/or architecture for a programmable transmit SCSI equalization device that may (i) provide controlled rise time and/or (ii) provide synchronized buffers for precompensation.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a conventional SCSI ULVD driver;

FIG. 2 is a block diagram of a preferred embodiment of the present invention;

FIG. 3 is a block diagram of an alternate embodiment of the present invention;

FIG. 4 is a block diagram of an exemplary implementation of the present invention;

FIG. 5 is a block diagram of a clock generation circuit in conjunction with the present invention;

FIG. 6 is a timing diagram of the circuit of FIG. 5;

FIG. 7 is a timing diagram of an operation of typical bandwidth effects over a transfer medium without pre-emphasis;

FIG. 8 is a timing diagram of an operation of the present invention;

FIG. 9 is a block diagram of an alternate embodiment of the present invention; and

FIG. 10 is a block diagram of a timing circuit of the circuit of FIG. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 2, a block diagram of circuit (or device) 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented as a small computer systems interface (SCSI) universal low voltage differential (ULVD) transceiver. The circuit 100 may provide a SCSI ULVD driver with precompensation and rise time control. The circuit 100 may be implemented to control rise and fall times with phased data. For example, the circuit 100 may provide controlled rise time of low voltage differential signals in a SCSI ULVD buffer. The circuit 100 may be configured to provide minimized rise time variation of differential drivers over process, voltage, and temperature corners. Additionally, the present invention may provide synchronization of multiple differential drivers (to be described in connection with FIGS. 3 and 4).

The circuit 100 generally comprises a circuit (or device) 102, a circuit (or device) 104, a current source 106, a current source 108, a terminator 110, and an inverter 112. The circuit 100 may also have an output pin (e.g., V+) and an output pin (e.g., V–). The circuit 102 generally comprises a number of parallel switches (e.g., A) and a number of parallel switches (e.g., C). The parallel switches A<1:N> and the parallel switches C<1:N> may be driven by a data signal (e.g., DATA). The data signal DATA may be a phased data signal with N phases, where N is a positive integer. The circuit 104 generally comprises a number of parallel switches (e.g., B) and a number of parallel switches (e.g., D). The parallel switches B<1:N> and the parallel switches D<1:N> may be driven by a complement of the phased data signal DATA. A number of each of the parallel switches A, B, C and D may be varied in order to meet the criteria of a particular implementation.

The switches A, B, C and D may be implemented as ULVD rise time control switches. The circuit 100 may implement rise time control by implementing N parallel switches (e.g., the switches A<1:N>, B<1:N>, C<1:N> and D<1:N>) driven by a phased data signal (e.g., the signal DATAN). The circuit 100 may break the output switches A, B, C and D in to multiple segments and drive them with the multiphase data signal DATAN. The timing between a first and a last data phase (e.g., DATA1 and DATAN) of the signal DATA may determine rise and fall times of an output differential waveform on the pins V+ and V–. The switches A, B, C and D may also be weighted to influence a pulse shape of the differential waveform.

Referring to FIG. 3, a block diagram of a circuit 180 illustrating an exemplary embodiment of the circuit 100 is shown. The circuit 180 may be similar to the circuit 100. The circuit 180 may be configured to synchronize multiple buffers. The circuit 180 may allow phased data to be created from a centrally generated phased clock. The circuit 180 may also allow two differential devices to become synchronized by a common phased clock (to be discussed further in connection with FIG. 4). The circuit 180 may additionally comprise a flip-flop 150 and a flip-flop 152. The flip-flops 150 and 152 may be implemented as output driver switches. The FF 150 may receive a signal (e.g., I1). The FF 152 may receive a signal (e.g., I1b). The FFs 150 and 152 may also receive a clock signal (e.g., CLOCK). The clock signal CLOCK may be implemented as a multiphase clock signal.